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EXAMINER	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/797,507	BOOR, STEVEN E.	
	Examiner	Art Unit	
	Fatimat O. Olaniran	4178	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-24 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-24 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 10 March 2004 is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date All.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

1. Claims 4-5 and 13 are objected to because of the following informalities: limitation "the circuit" lacks antecedent basis. For purposes of writing this report examiner assumes "the circuit' refers to the tuning circuit. Appropriate correction is required.

Double Patenting

2. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent either is shown to be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement.

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

3. Claims 15-24 are provisionally rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 1-9, 11-12 and 14-16 of copending Application No. 10797804. This is a provisional obviousness-type

double patenting rejection because the conflicting claims have not in fact been patented.

Application claim 15 and co-pending Application claim 1 (10797804) are both drawn to the same invention. These claims differ in scope in that application claim 15 is broader in scope than co-pending Application claim 1 (10797804). Therefore it would have been obvious to one of ordinary skill in the art, at the time the invention was made to modify co-pending Application (10797804) by omitting some limitations so as to obtain claim 15 as claimed.

Allowance of claim 15 would result in an unjustified time-wise extension of the monopoly granted for the invention defined by co-pending Application claim 1. Therefore, provisional obviousness-type double patenting is appropriate because the conflicting claims have not in fact been patented.

Claim 16 corresponds to co-pending application 10797804 claim 2

Claim 17 corresponds to co-pending application 10797804 claim 3

Claim 18 corresponds to co-pending application 10797804 claims 4, 5, 6, 7 and 8

Claim 19 corresponds to co-pending application 10797804 claim 9

Application claim 20 and co-pending Application claim 11 (10797804) are both drawn to the same invention. These claims differ in scope in that application claim 20 is broader in scope than co-pending Application claim 11 (10797804). Therefore it would have been obvious to one of ordinary skill in the art, at the time the invention was made

to modify co-pending Application (10797804) by omitting the limitation so as to obtain claim 20 as claimed.

Allowance of claim 20 would result in an unjustified time-wise extension of the monopoly granted for the invention defined by co-pending Application claim 11. Therefore, provisional obviousness-type double patenting is appropriate because the conflicting claims have not in fact been patented.

Claims 21 corresponds to application 10797804 claim 11

Claim 22 corresponds to application 10797804 claim 12

Claim 23 corresponds to application 10797804 claim 14

Claim 24 corresponds to application 10797804 claims 15 and 16

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 1, 9-10, 12-13, 15-16, and 19-20 are rejected under 35 U.S.C. 102(b) as being anticipated by Levitt et al. (4879749).

Claim 1 Levitt discloses a buffer circuit (Fig. 1, Fig. 2) for use in a microphone assembly comprising:

an input for receiving a signal (Fig. 2: microphone 57); an input buffer (Fig. 2; element 58 PROGR AGC) coupled to the input; an output (col. 5 line 7-11); a filter network

coupled (Fig. 2: element 64) between the input buffer and the output; a selector (Fig. 1;host controller col. 3 line 36, Fig. 2; 84: EEPROM) comprising: a first input (col. 4 line 30-33 output host controller); a first output responsive to the first input (col. 2 line 49-51output EEPROM); and a tuning circuit (Fig. 2; 84 :EEPROM, tri-state switches, 85-86) coupled to the filter network for adjusting a characteristic of the filter network (col. 2 line 49-51), the tuning circuit responsive to the selector (col. 5 line 36-37), wherein the characteristic of the filter network is adjusted using the first input (col. 5 line 36-37).

Claim 2 Levitt discloses, wherein the first input is on a separable tab (Fig. 1:124, EEPROM programming socket, col. 8 line 25-29).

Claim 9, Levitt discloses, wherein the first input is coupled to a biasing element (col. 5 line 34-37).

Claim 10, Levitt discloses, wherein the biasing element maintains a persistent state responsive to a programming signal applied to the first input (col. 5 line 34-37).

Claim 12, Levitt discloses wherein the biasing element is an EEPROM (col. 5 line 34-37).

Claim 13 analyzed with respect to claim 1, Levitt further discloses a resistive element coupled between the filter network and the circuit (Fig. 2 element 86, tri-state switch).

Claim 15, Levitt discloses a hybrid circuit for buffering (Fig. 2) an audio signal comprising: a substrate having a first (Fig. 2) and second portion (Fig. 1), the second portion severable from the first portion (Fig. 1:124, EEPROM programming socket); and a buffer circuit substantially disposed on the first portion of the substrate, the buffer circuit comprising: a first input for coupling the audio signal (Fig. 2:element 57, microphone); a filter network coupled to the first input (Fig. 2, element 64); an output coupled to the filter network (Fig. 2, col. 5 line 7-11); a tuner for adjusting the filter network (Fig. 2:EEPROM); and a controller for altering a value of the tuner (Fig. 1 host controller), the controller having a second input, the second input disposed on the second portion of the substrate (Fig. 1 element 24, input from computer), whereby a tuning signal coupled to the second input is used to adjust the tuner (col. 4 line 38-43), thereby changing a transfer function of the buffer circuit (col. 4 line 30-33).

Claim 16, Levitt discloses wherein the controller retains a setting upon receiving the tuning signal (col. 4 line 38-43).

Claim 19, Levitt discloses wherein the second input is further coupled to a biasing element, the biasing element maintaining a state after receiving the tuning signal (col. 5 line 34-37).

Claim 20 Levitt discloses, A method for adjusting a buffer circuit for use in a microphone assembly comprising:

providing a desired response characteristic for the buffer circuit (col. 6 line 65-67); measuring an initial response characteristic of the buffer circuit (col. 6 line 68); comparing the desired response characteristic to the initial response characteristic (col. 7 line 1-2); determining an adjustment using the comparison, the adjustment for reducing a difference between the desired and initial response characteristics (col. 7 line 1-2); transmitting a signal to a selector circuit in the buffer circuit (col. 7 line 6-8); and tuning an adjustable filter coupled to the selector circuit (col. 7 line 11-12), the adjustable filter for modifying the initial response characteristic (col. 7 line 65-67).

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claim 3, 14,17 and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Levitt et al (4879749).

Claim 3 analyzed with respect to claim 1, Levitt discloses, wherein the first input is on a separable tab (Fig. 1:124, EEPROM programming socket) and the characteristic of the filter network (col. 5 line 38-40) is adjusted (col. 8 line 25-29). Levitt does not clearly disclose wherein the first input is on a separable tab and the separable tab is removed

from the buffer circuit after the characteristic of the filter network is adjusted. However it would be obvious to one ordinarily skilled in the art at the time the invention was made to place the host controller on a separable tab so that the buffer circuit can be removed from the programming device after programming and so user will not have to use the microphone assembly with an additional circuit or device attached.

Claim 14 analyzed with respect to claim 13 and claim1, Levitt does not clearly disclose wherein a value of the resistive element is 500k ohms. However, it would be obvious to one of ordinarily skill in the art at the time the invention was made to set the value of the resistive element to 500k ohms in the course of circuit design so as to limit current applied or as necessary.

Claim 17 Levitt analyzed with respect to claim 15, Levitt discloses, wherein the second portion of the substrate (Fig. 1:124, EEPROM programming socket) and the controller receives the tuning signal (col. 8 line 25-29). Levitt does not clearly disclose wherein the second portion of the substrate is permanently removed after the controller receives the tuning signal. However, it would be obvious to one ordinarily skilled in the art at the time the invention was made to permanently remove the programming device from the buffer circuit so that the circuit can perform the function it was programmed to without having an additional circuit attached.

Claim 22 analyzed with respect to claim 20, Levitt discloses transmitting the signal to the selector circuit (col. 8 line 25-29). Levitt does not clearly disclose removing a portion of the buffer circuit used in transmitting the signal to the selector circuit. However, it would be obvious to one ordinarily skilled in the art at the time the invention was made to permanently remove the programming device, (which has the portion for transmitting the signal to the selector circuit), from the buffer circuit so that the circuit can perform the function it was programmed to without having an additional circuit attached.

8. Claim 4-8, 18 and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Levitt et al (4879749) in view of Killion (5602925)

Claim 4 analyzed with respect to claim 1, Levitt does not disclose wherein the circuit comprises a resistor network.

Killion discloses wherein the circuit comprises a resistor network (Figs. 6). Therefore it would be obvious to one ordinarily skilled in the art at the time the invention was made to modify the circuit of Levitt with the resistor network of Killion in order to have at least one programmable resistor for setting the audio response of the hearing aid as taught by Killion (abstract line 1-3).

Claim 5 analyzed with respect to claim 1, Levitt does not disclose wherein the circuit is a ladder network, the ladder network adjustable by activating a semiconductor device between an element of the ladder network and a ground connection. Killion discloses wherein the circuit is a ladder network (Fig. 6), the ladder network adjustable by

activating a semiconductor device between an element of the ladder network and a ground connection (Fig. 6 col. 6 line 7-9). Therefore it would be obvious to one ordinarily skilled in the art at the time the invention was made to modify the circuit of Levitt with the ladder network and semiconductor of Killion in order to save space when implementing the circuit and in order to have a silicon based switch that can be implemented with the rest of the circuit.

Claim 6 analyzed with respect to claim 5 and claim 1, Killion further discloses wherein the ladder network comprises one of resistors and capacitors (Fig 6).

Claim 7 analyzed with respect to claim 6, claim 5, and claim 1, Killion does not clearly disclose discloses wherein a resistor of the ladder network has a value of 5.5k ohms. However, it would be obvious to one of ordinarily skill in the art at the time the invention was made to set the value of the resistive element to 5.5k ohms in the course of circuit design so as to limit current applied or as necessary.

Claim 8 analyzed with respect to claim 5 and claim 1, Killion further discloses wherein the semiconductor device is a field effect transistor (FET) (Fig.6. col. 6 line 7-9).

Claim 18 analyzed with respect to claim 15, Levitt does not disclose wherein the tuner is a ladder network adjustable by activating a semiconductor device between an element

of the ladder network and a ground network. Killion discloses wherein the tuner is a ladder network adjustable by activating a semiconductor device between an element of the ladder network and a ground network (Fig. 6. col. 6 line 7-9). Therefore it would be obvious to one ordinarily skilled in the art at the time the invention was made to implement the tuner of Levitt as a ladder network with a semiconductor in order to have a circuit that can be implemented on a chip.

Claim 23, Levitt discloses tuning the adjustable filter (col. 5 line 3-7) Levitt does not disclose, further comprises activating a semiconductor device between an element of a ladder network and a ground connection. Killion discloses activating a semiconductor device between an element of a ladder network and a ground connection (Fig. 6 col. 6 line 7-9). Therefore it would be obvious to one ordinarily skilled in the art at the time the invention was made to modify the circuit of Levitt with the ladder network and semiconductor of Killion in order to save space when implementing the circuit and in order to have a silicon based switch that can be implemented with the rest of the circuit.

9. Claim 11, 24 are rejected under 35 U.S.C. 103(a) as being unpatentable Levitt et al (4879749) in view of Advani et al. (4926459).

Claim 11 analyzed with respect to claim 1, 9, and 10. Levitt does not disclose wherein the biasing element is a zener-zap diode. Advani discloses wherein the biasing element is a zener-zap diode (Fig. 3; element 106, col.7 line 46-47). Therefore it would be obvious to one ordinarily skilled in the art at the time the invention was made to modify

the circuit of Levitt with a zener-zap diode in order to utilize the breakdown characteristic of diodes.

Claim 24 analyzed with respect to claim 20, Levitt discloses tuning the adjustable filter (col. 5 line 3-7). Levitt does not disclose further comprises biasing the selector circuit with a zener-zap diode. Advani discloses further comprises biasing the circuit with a zener-zap diode (Fig. 3; element 106, col.7 line 46-47). Therefore it would be obvious to one ordinarily skilled in the art at the time the invention was made to modify the circuit of Levitt with a zener-zap diode in order to utilize the breakdown characteristic of diodes.

10. Claim 21 is rejected under 35 U.S.C. 103(a) as being unpatentable over Levitt et al (4879749) in view of Madaffari et al. (2002/0090102)

Claim 21 Levitt discloses a portion of the buffer circuit accessible from outside the housing (Fig. 1:element 24 col. 4 line 29). Levitt does not disclose assembling the buffer circuit in acoustically sealed housing. Madaffari discloses assembling the buffer circuit in acoustically sealed housing (Fig. 2 paragraph 15 line 13-15). Therefore it would be obvious to one ordinarily skilled in the art at the time the invention was made to modify the circuit of Levitt with the housing of Madaffari in order to protect the circuit from EMI and other interferences.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Fatimat O. Olaniran whose telephone number is 571-270-3437. The examiner can normally be reached on M-F Alt F off 8:30-5 EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Hai Tran can be reached on 571-272-7305. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

FO

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PRIMARY EXAMINER